REMARKS/ARGUMENTS

In the above-identified Office Action, the Examiner objected to claims 1, 9, 17, 26, and 37, and rejected claims 1-26 and 28-39 under 35 U.S.C. §103(a). These objections and rejections are fully traversed below.

Claims 1, 7, 9, 17, 25, 26 and 37 have been amended to further clarify the subject matter regarded as the invention. Claim 15 is hereby cancelled without prejudice. Claims 1-26 and 28-39 remain pending in this application.

Reconsideration of the application is respectfully requested based on the amendments and the following remarks.

CLAIM OBJECTIONS

In the Office Action, claims 1, 9, 17, 26 and 37 were objected to due to formatting informalities. These claims have been amended to correct these informalities. Accordingly, it is respectfully requested that the Examiner withdraw the objection to claims 1, 9, 17, 26 and 37.

REJECTION OF CLAIMS 1-26 AND 28-39 UNDER 35 U.S.C. §103

In the Office Action, the Examiner rejected claim 1-8 under 35 U.S.C. §103(a) as being unpatentable over Bartley (U.S. Patent No. 6,219,796) in view of Fletcher et al. (U.S. Patent No. 6,611,920); rejected claims 9-16 over Bartley in view of Fletcher and Matter et al. (U.S. Patent No. 5,392,437); rejected claim 17-25 over Matter et al. in view of Bartley, Fletcher and Sproch et al. (U.S. Patent No. 6,247,134); rejected claims 26 and 28-36 over Bartley in view of Fletcher and Sproch et al.; rejected claim 37 over Matter in view of Bartley, Fletcher and Sproch et al.; and rejected claim 39 over Bartley, Fletcher, and Simonvich (U.S. Patent 6,308,241). These rejections are traversed below.

The present invention pertains to methods and systems for saving power in pipelined processors. **Claims 1-8** will be addressed first. Specifically, claim 1 of the present invention requires the controlling of the supply of current to each of a plurality of stages of a functional unit after evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. The method of claim 1 allows for efficient evaluation of operation type of each instruction so that power supplied to each stage of a functional unit can be individually controlled.

Among other things, claim 1 recites:

"**producing activity indicators** **by reading an operation type from an instruction and providing an associated signal comprising one of a clock marker or a no-clock marker** based upon the operation types of said instructions;"

and

"following said steps of evaluating said instructions and producing said activity indicators, controlling the supply of current to each of said plurality of stages **by providing a clock signal and the activity indicators to a logic gate that determines** ~~such~~"

Bartley pertains to optimizing a computer program to provide better power management for microprocessors. Bartley operates to optimize computer code to insert "power-down" instructions for a functional unit when such is not needed. The power-related instructions are added manually by a programmer or by a compiler or assembler. See col. 7, lines 31-38. Here, the computer code is being altered. Hence, **Bartley does not produce activity indicators** as recited in claim 1. Furthermore, claim 1 pertains to instructions that are executed by a series arrangement of stages of a functional unit. Significantly, Bartley also **does not teach or suggest use of a multi-stage functional unit or individually controlling stages of a multi-stage functional unit.**

Fletcher pertains to a power control system in which a functional unit block can have stages that are separately powered. Presumably, powering of the stages is based on a valid indicator signal that is received by the functional unit block when valid data is input. Even so, in contrast to claim 1, Fletcher fails to provide any teaching or suggestion towards evaluating instructions to determine operation type and then producing activity indicators based upon the operation types of the instructions. Importantly, Fletcher is also deficient that it also does not generate **activity indicators.** Therefore, Fletcher et al. fails to teach or suggest **producing activity indicators** or the controlling of the supply of current to each of a plurality of stages of a functional unit following the evaluating of instructions and producing of activity indicators.

Accordingly, it is submitted that Bartley and Fletcher alone or in any combination, do not teach or suggest all the features of claim 1. In addition, it is submitted that dependent claims 2-8, are also patentably distinct from cited art for at least the same reasons as those recited above for independent claim 1. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the

claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-8.

Claims 9-16 and Claim 39 are also traversed. Independent claim 9 and dependent claim 39 of the present invention pertain to methods that require receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. The instruction register temporarily stores instructions before they are executed. As recited in claims 9 and 39, the instructions are evaluated for their operation type shortly before being executed. Depending on the operation types, the instructions can be executed by the plurality of stages of the functional unit, where the stages are arranged in series. In contrast, neither Bartley nor Fletcher et al. teach or suggest receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. Matter et al. discloses an instruction cache which may, at best, correspond to an instruction register of claims 9 and 39; however, there is no teaching or suggestion of an instruction evaluation unit that receives instructions from the instruction register for evaluation. Additionally, the cited art **does not teach a shift register** as claimed. Therefore, it is submitted that Bartley, Fletcher et al. and Matter et al., alone or in any combination, do not teach or suggest the features of claims 9 and 39. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 9-14, 16 & 39.

Claims 17-25 and 37 pertain to a microprocessor and system where an instruction evaluation unit is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Furthermore, independent claims 17 and 37 recited that a **stage activation controller is connected to the instruction evaluation unit,** wherein the stage activation controller utilizes the **activity indicators** to activate or deactivate each stage of a multi-stage functional unit. In contrast, neither Bartley nor Fletcher et al. teach or suggest an instruction evaluation unit that is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Moreover, as discussed above, Matter does not teach an instruction register either. Also, neither Bartley nor Fletcher et al. teach or suggest a stage activation controller that is connected to the instruction evaluation unit.

The applicants also point out that the cited art does not teach "activity indicators" nor does the cited art teach generating "activity indicators by reading an operation type from the

instruction and providing an associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of said instructions". Also, the cited art does not teach a "stage activation controller that is connected to said instruction evaluation unit and includes logic gates that utilize ... said activity indicators in conjunction with a stage activation clock pulse of a clock signal to determine which of said stages are to be activated or deactivated".

Therefore, it is submitted that the cited references, alone or in any combination, do not teach or suggest the features of claims 17 and 37. The applicants do not at this time discuss the additional limitations recited in the dependent claims, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. However, the applicants point out in passing that, for example, as to Claim 25 the cited art does not teach "**logic gates of the stage activation controller comprise AND type gates**". Accordingly, it is respectfully requested that the Examiner withdraw the rejections of claims 17-25 & 39.

Claims 26 and 28-35 pertain to microprocessors that include an instruction evaluation unit and a stage activation controller. The instruction evaluation unit evaluates a next instruction to be executed and produces activity indicators. The stage activation controller utilizes the activity indicators to activate or deactivate each stage of a multi-stage functional unit. In contrast, neither Bartley nor Fletcher et al. teach or suggest an instruction evaluation unit, a stage activation controller, or an instruction evaluation unit as recited in claim 26.

In further evaluating Claim 26, the Action argues that Bartley teaches "an **instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators**". Bartley teaches a decoder and dispatcher that get information from fetch packets that is used by the system. They don't produce or generate anything as does the claimed invention which uses the operation type to produce an activity indicator. This activity indicator is then processed together with a clock signal through a logic gate to determine whether the functional stage operates at a given time. Sproch adds nothing to this argument. Therefore, it is submitted that Bartley, Fletcher et al. or Sproch et al., alone or in any combination, do not teach or suggest the features of, for example, claim 26.

Based on the foregoing, it is submitted that claims 1, 9, 17, 26 and 37 are patentably distinct from Bartley, Fletcher et al., Matter et al., Sproch et al. and/or Simonvich. In addition, it is submitted that dependent claims 2-8, 10-14, 16, 18-25, 28-36, 38-39 are also patentably distinct from Bartley, Fletcher et al., Matter et al., Sproch et al. and/or Simonvich for at least the same reasons as those recited above for their corresponding independent claims. The additional

limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-14, 15-26, and 28-39 under 35 U.S.C § 103(a).

Putting aside the fact that the references generally do not teach or suggest the claimed invention, the asserted grounds for rejection are deficient for other reasons. In particular, "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings ... The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant"s disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). **"To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). In the present case, the suggestion to combine has been arrived at using the teachings of the pending allocation. Accordingly, the suggestion to combine is an impermissible hindsight application of a hindsight teaching. Absent the teachings of the present application, there is no suggestion in any of the cited references indicating that they should be combined.**

In view of the foregoing, the cited references fail to establish a prima facie case of obviousness as to the rejected claims. So for this added reason it is believed that the claimed invention is patentable over the art of record. .

SUMMARY

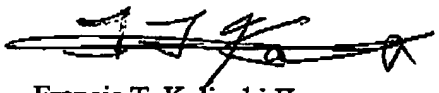
It is submitted that the objections to claims 1, 9, 17, 26 and 37 have been overcome. In addition, it is submitted that claims 1-14, 16-26 and 28-39 are patentable distinct from any combination of the cited art relied on by the Examiner. Therefore, it is submitted that claims 1-14, 16-26, and 28-39 are patentably distinct from the cited references. Reconsideration of the application and an early Notice of Allowance are earnestly solicited.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. APL1P203).

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



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